

CMOS VLSI Design

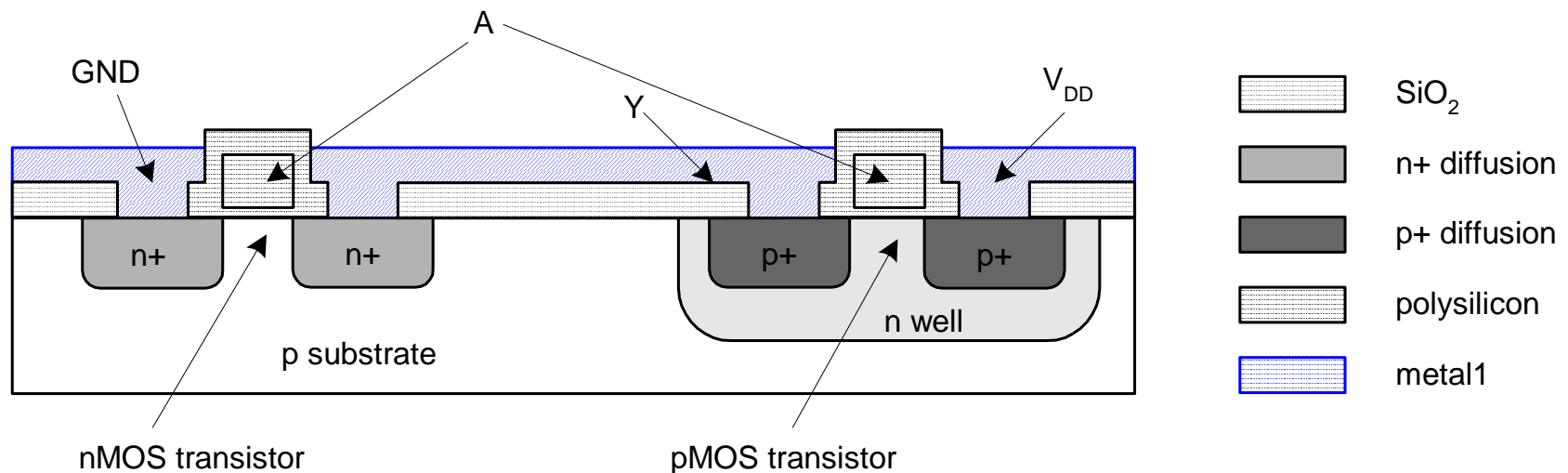
Fabrication and Layout

CMOS Fabrication

- ❑ CMOS transistors are fabricated on silicon wafer
- ❑ Lithography process similar to printing press
- ❑ On each step, different materials are deposited or etched
- ❑ Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

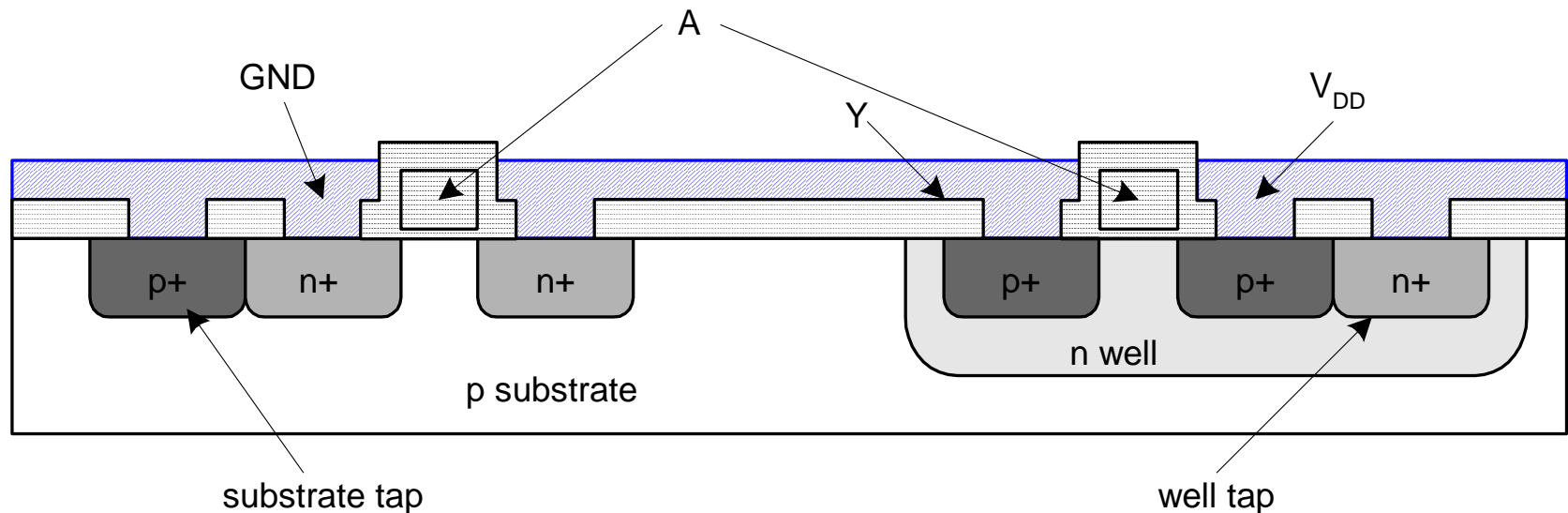
Inverter Cross-section

- Typically use p-type substrate for nMOS transistor
 - Requires n-well for body of pMOS transistors
 - Several alternatives: SOI, twin-tub, etc.



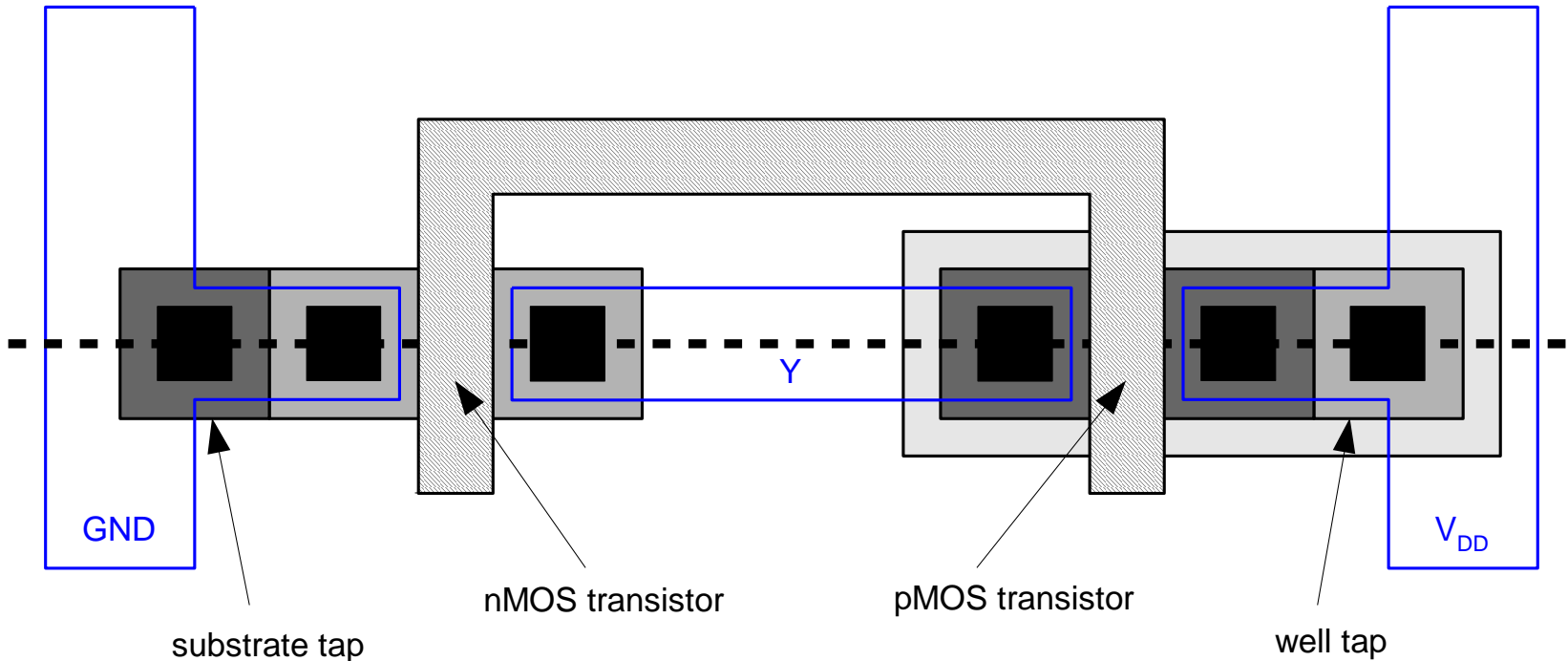
Well and Substrate Taps

- ❑ Substrate must be tied to GND and n-well to V_{DD}
- ❑ Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- ❑ Use heavily doped well and substrate contacts / taps



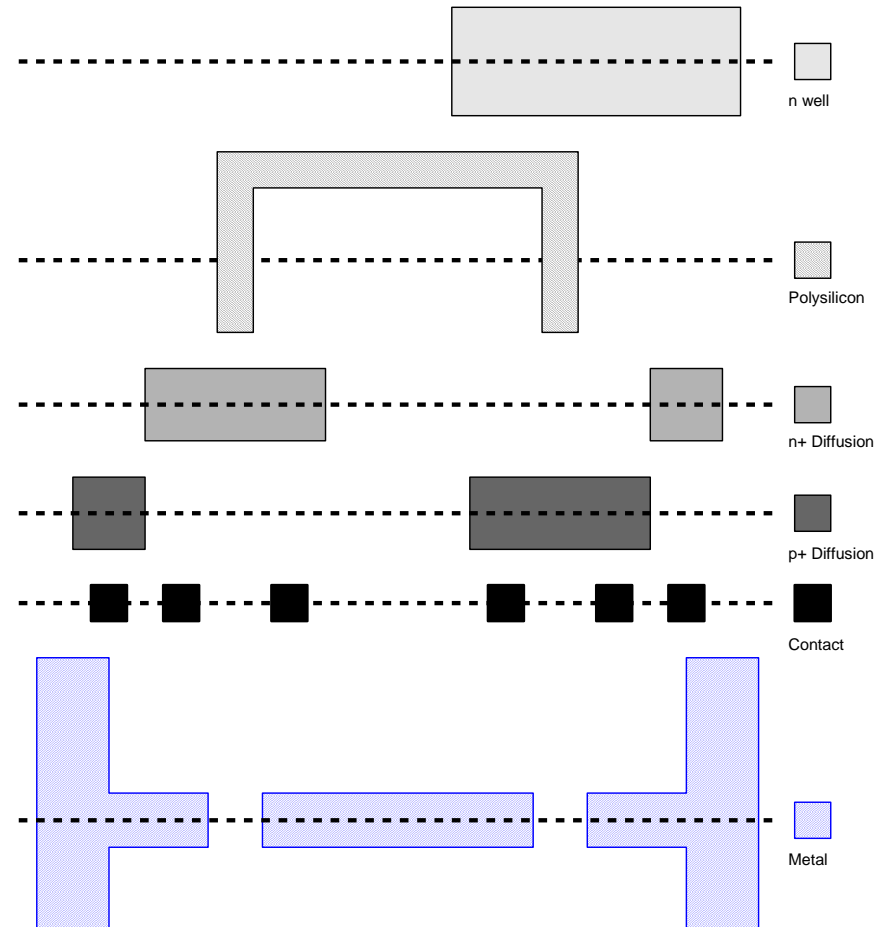
Inverter Mask Set

- ❑ Transistors and wires are defined by *masks*
- ❑ Cross-section taken along dashed line



Detailed Mask Views

- ❑ Six masks
 - n-well
 - Polysilicon
 - n+ diffusion
 - p+ diffusion
 - Contact
 - Metal



Fabrication Steps

- ❑ Start with blank wafer
- ❑ Build inverter from the bottom up
- ❑ First step will be to form the n-well
 - Cover wafer with protective layer of SiO_2 (oxide)
 - Remove layer where n-well should be built
 - Implant or diffuse n dopants into exposed wafer
 - Strip off SiO_2



p substrate

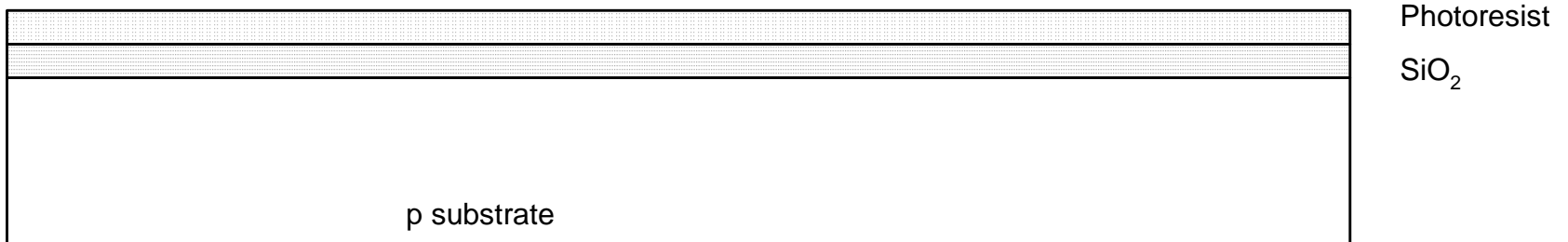
Oxidation

- ❑ Grow SiO_2 on top of Si wafer
 - 900 – 1200 C with H_2O or O_2 in oxidation furnace



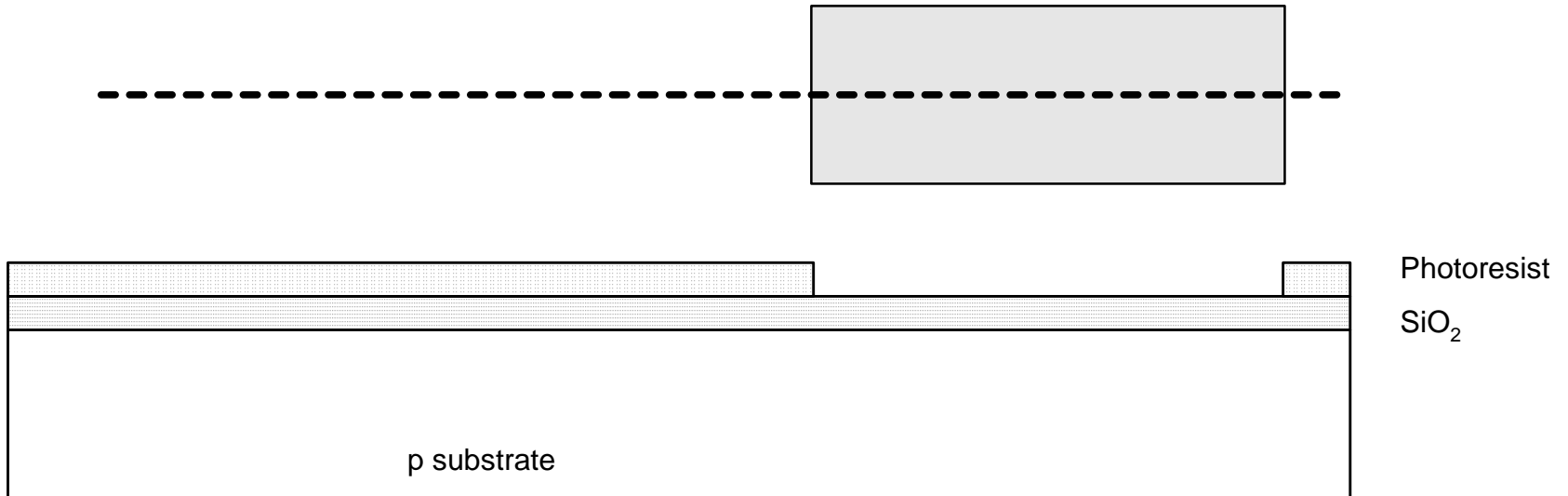
Photoresist

- ❑ Spin on photoresist
 - Photoresist is a light-sensitive organic polymer
 - Softens where exposed to light



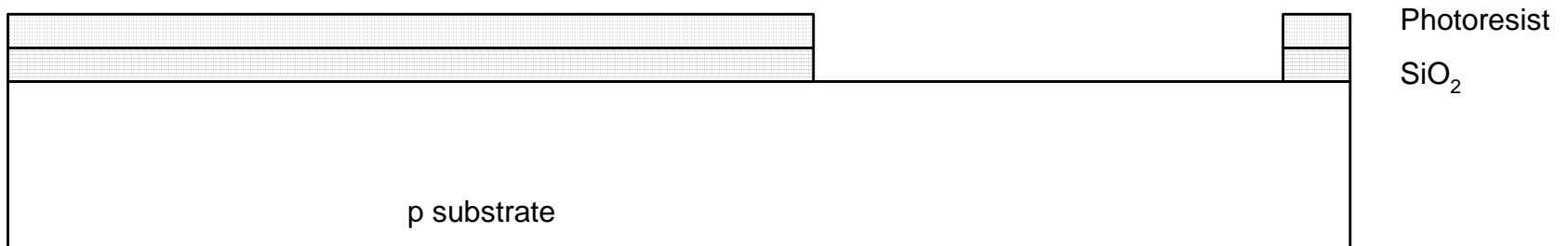
Lithography

- ☐ Expose photoresist through n-well mask
- ☐ Strip off exposed photoresist



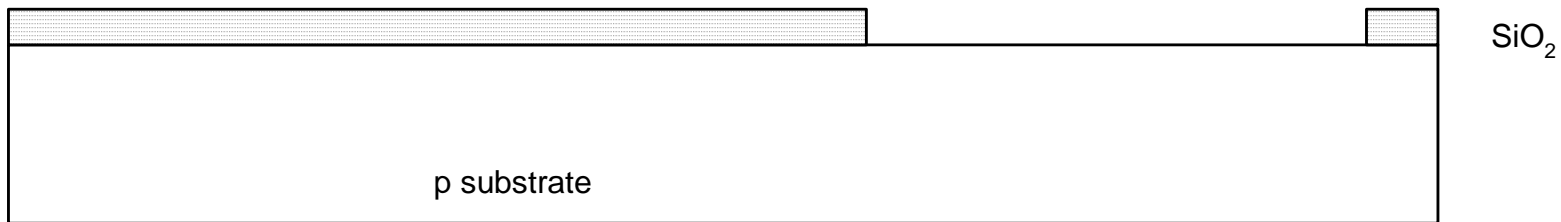
Etch

- ❑ Etch oxide with hydrofluoric acid (HF)
 - Seeps through skin and eats bone; nasty stuff!!!
- ❑ Only attacks oxide where resist has been exposed



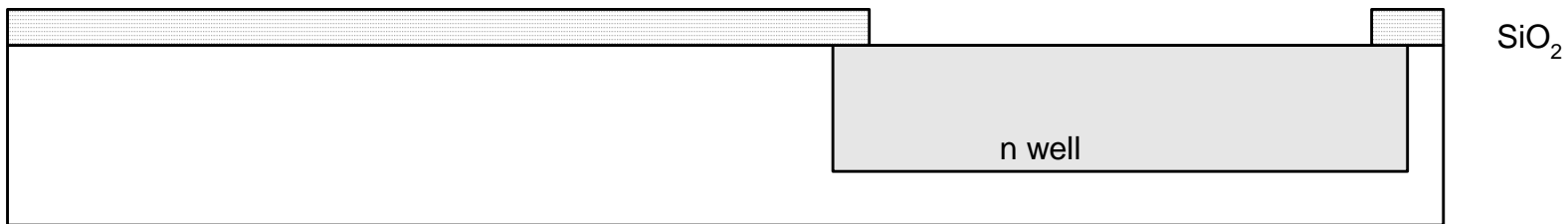
Strip Photoresist

- ❑ Strip off remaining photoresist
 - Use mixture of acids called piranah etch
- ❑ Necessary so resist doesn't melt in next step



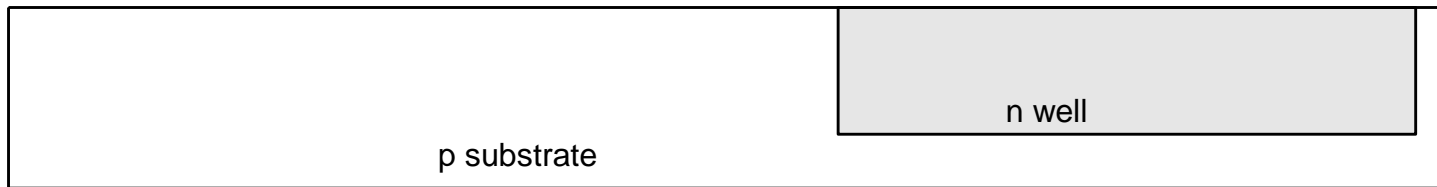
n-well

- ❑ n-well is formed with diffusion or ion implantation
- ❑ Diffusion
 - Place wafer in furnace with arsenic gas
 - Heat until As atoms diffuse into exposed Si
- ❑ Ion Implantation
 - Blast wafer with beam of As ions
 - Ions blocked by SiO_2 , only enter exposed Si



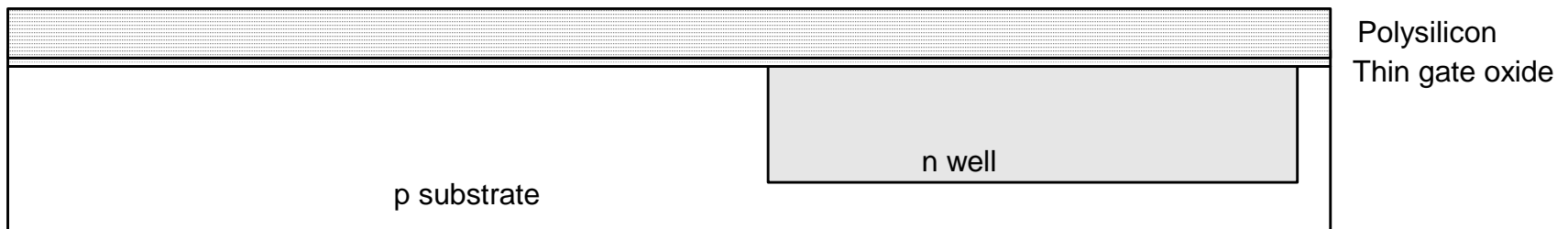
Strip Oxide

- ❑ Strip off the remaining oxide using HF
- ❑ Back to bare wafer with n-well
- ❑ Subsequent steps involve similar series of steps



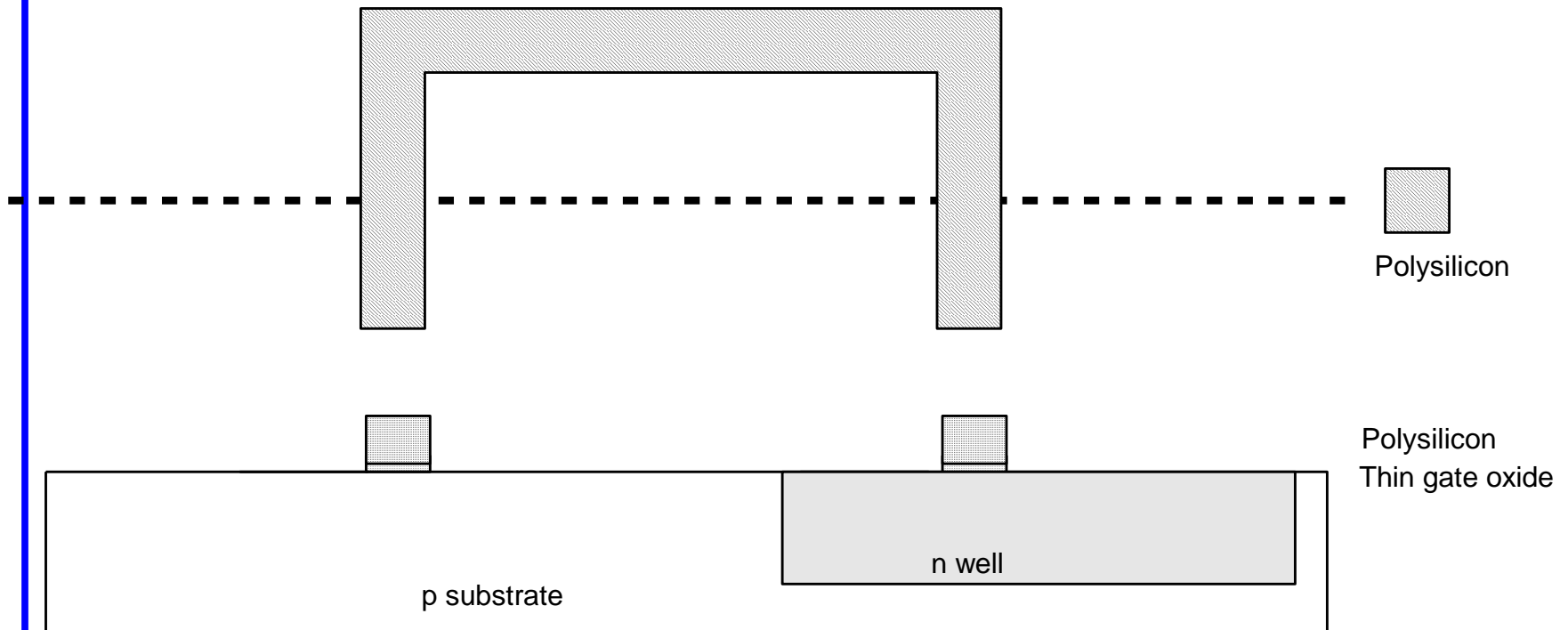
Polysilicon

- ❑ Deposit very thin layer of gate oxide
 - $< 20 \text{ \AA}$ (6-7 atomic layers)
- ❑ Chemical Vapor Deposition (CVD) of silicon layer
 - Place wafer in furnace with Silane gas (SiH_4)
 - Forms many small crystals called polysilicon
 - Heavily doped to be good conductor



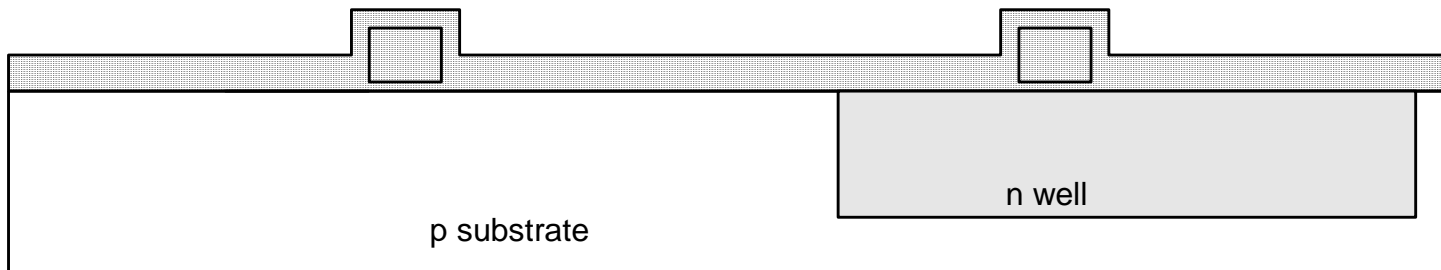
Polysilicon Patterning

- ❑ Use same lithography process to pattern polysilicon



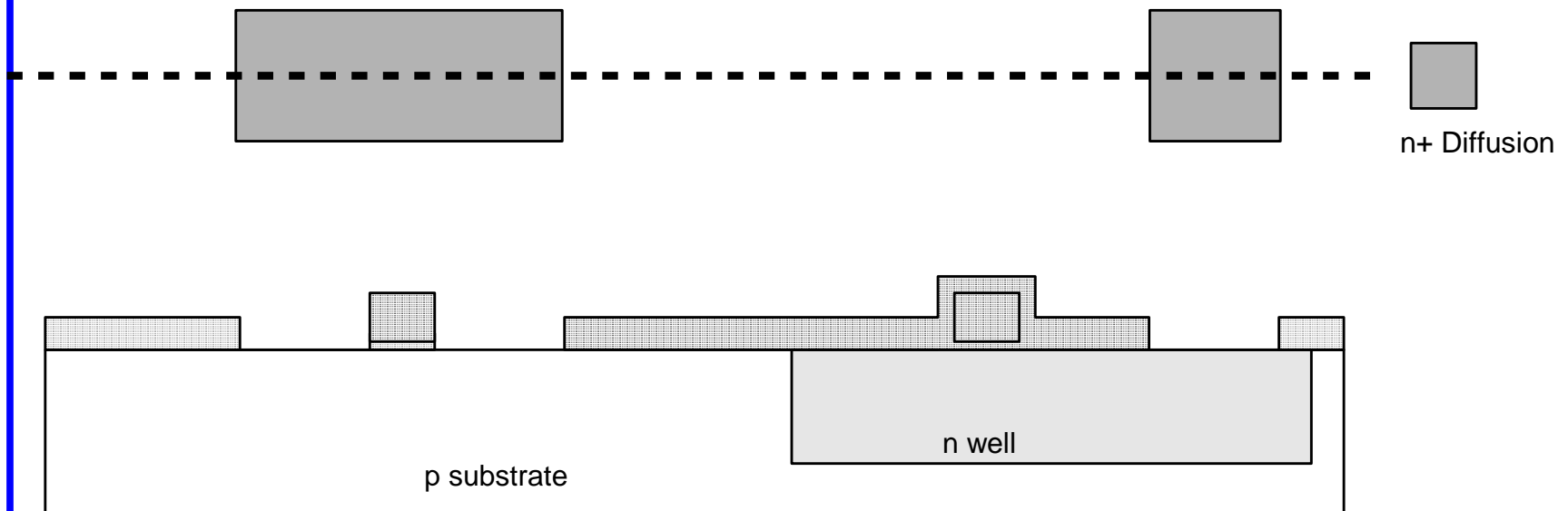
Self-Aligned Process

- ❑ Use oxide and masking to expose where n+ dopants should be diffused or implanted
- ❑ N-diffusion forms nMOS source, drain, and n-well contact



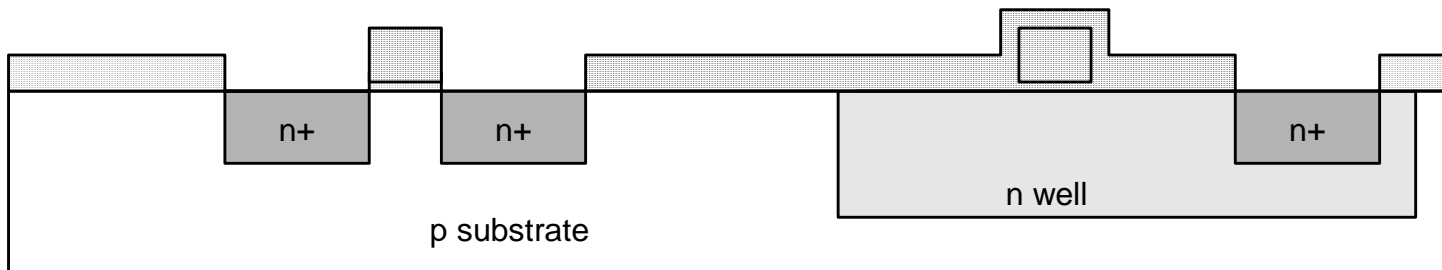
N-diffusion

- ❑ Pattern oxide and form n+ regions
- ❑ *Self-aligned process* where gate blocks diffusion
- ❑ Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



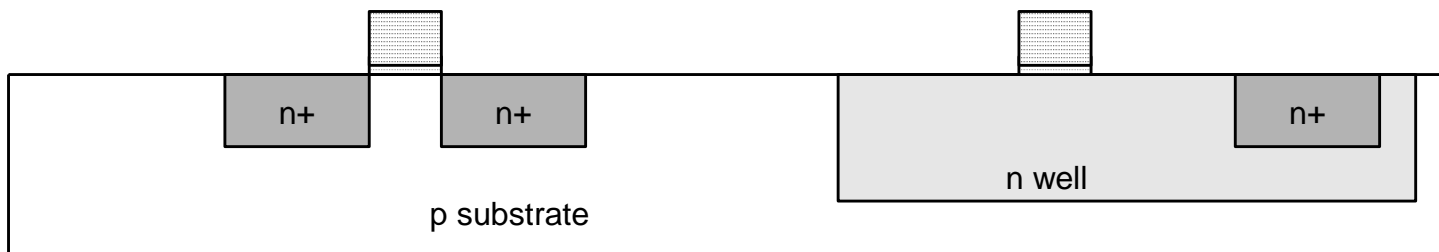
N-diffusion

- ❑ Historically dopants were diffused
- ❑ Usually ion implantation today
- ❑ But regions are still called diffusion



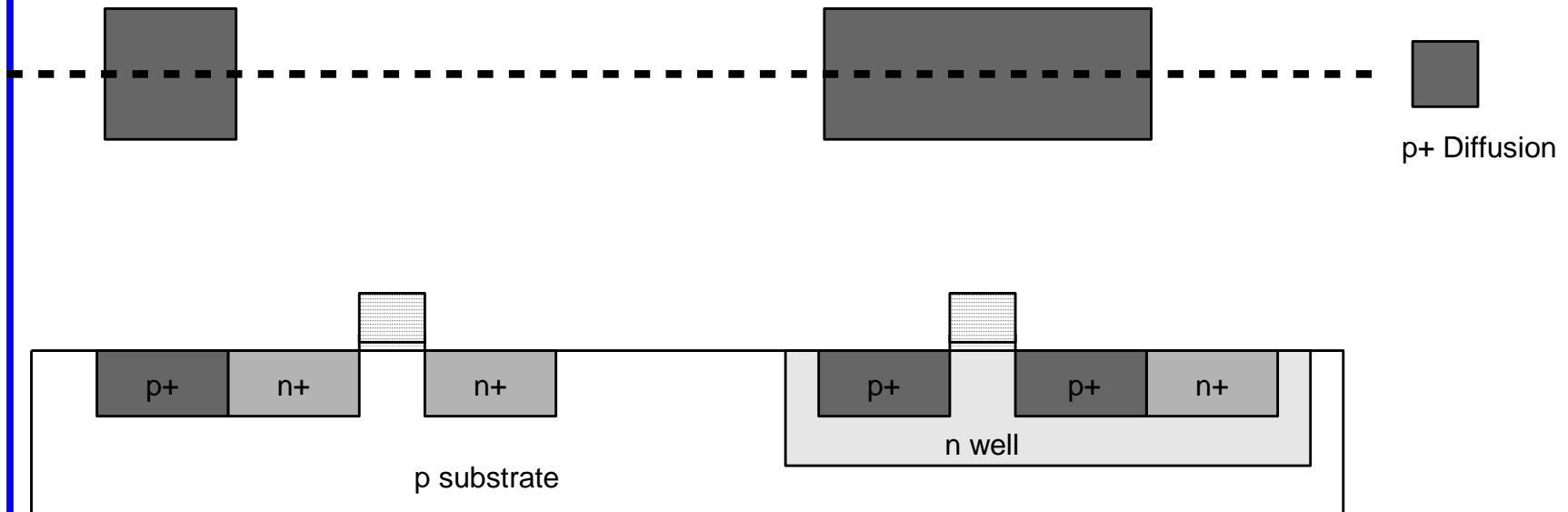
N-diffusion

- ❑ Strip off oxide to complete patterning step



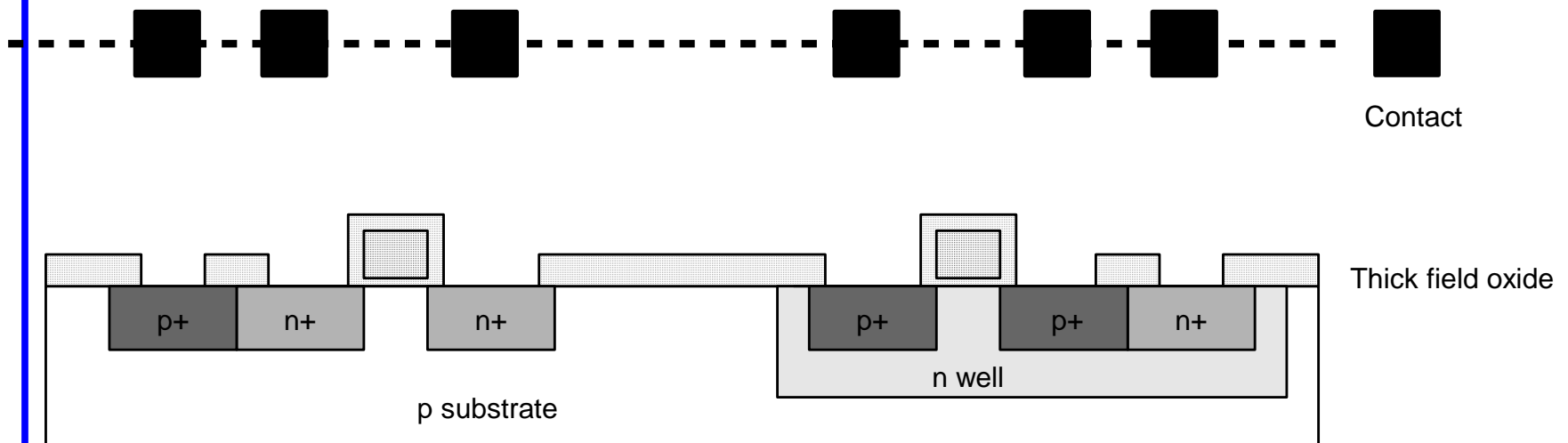
P-Diffusion

- ❑ Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



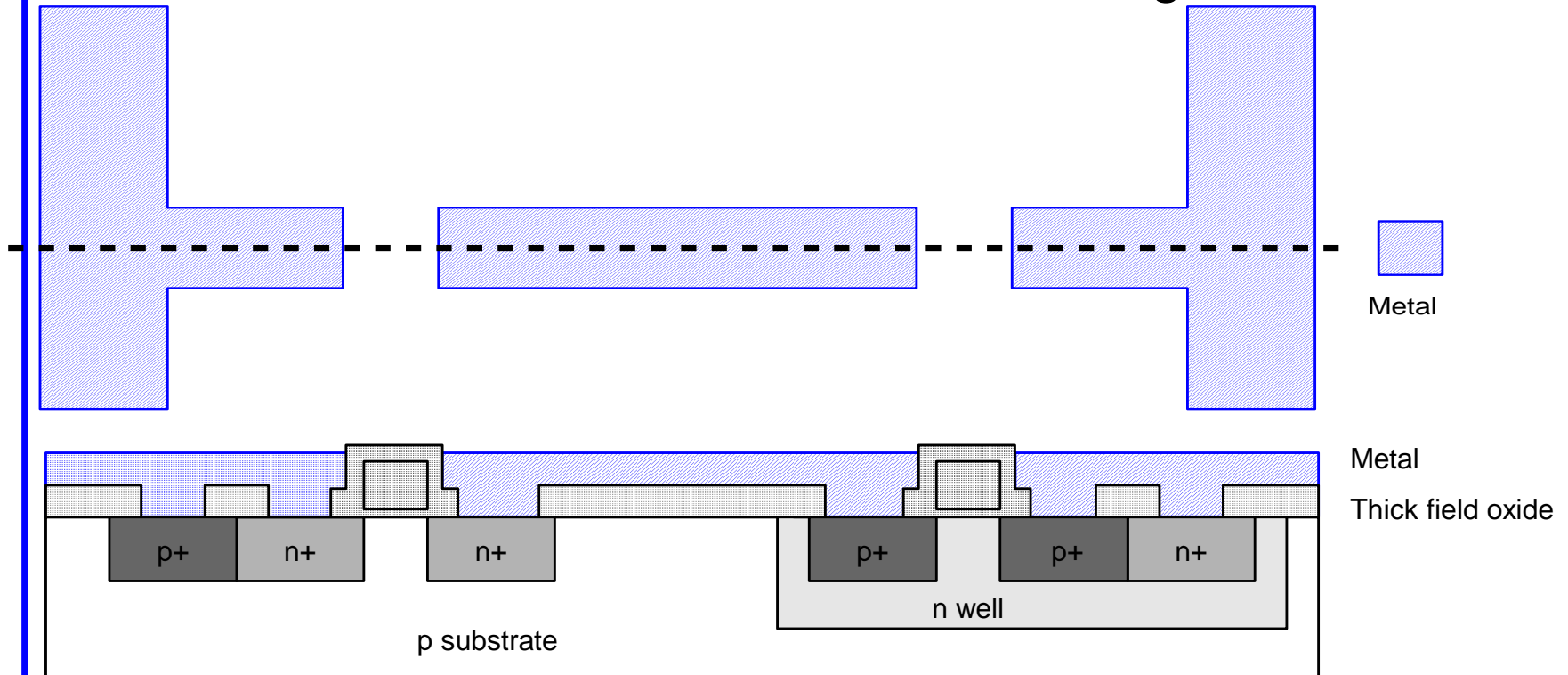
Contacts

- ❑ Now we need to wire together the devices
- ❑ Cover chip with thick field oxide
- ❑ Etch oxide where contact cuts are needed



Metallization

- ❑ Sputter on aluminum over whole wafer
- ❑ Pattern to remove excess metal, leaving wires



Layout

- ❑ Chips are specified with set of masks
- ❑ Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- ❑ Feature size f = distance between source and drain
 - Set by minimum width of polysilicon
- ❑ Feature size improves 30% every 3 years or so
- ❑ Normalize for feature size when describing design rules
- ❑ Express rules in terms of $\lambda = f/2$
 - E.g. $\lambda = 0.3 \mu\text{m}$ in $0.6 \mu\text{m}$ process

Set of Design Rules for Layout

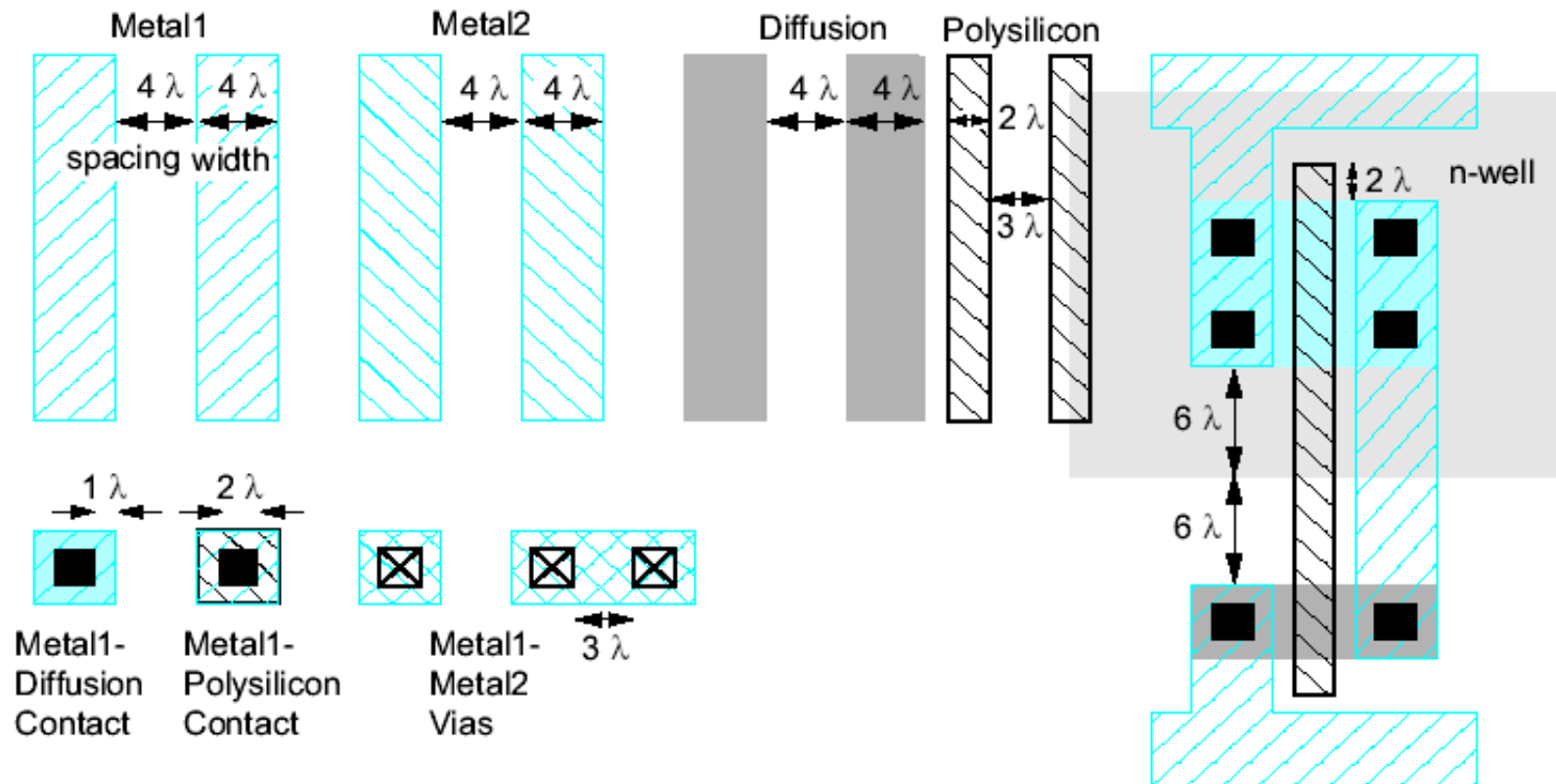
(with 2 metal layers in an m-layer process)

- ❑ Metal and Diffusion have minimum width and spacing of 4λ
- ❑ Contacts are $2\lambda \times 2\lambda$ surrounded by 1λ above and below
- ❑ Polysilicon uses a width of 2λ
- ❑ Polysilicon overlaps diffusion by 2λ where transistor is to be formed and a spacing of 1λ where no transistor
- ❑ Polysilicon and contacts have spacing of 3λ from other Polysilicon and contacts
- ❑ N-well surrounds pMOS transistors by 6λ and avoids nMOS transistors by 6λ

$\lambda = \text{channel length}/2$, e.g. $\lambda = 0.3 \mu\text{m}$ in $0.6 \mu\text{m}$ process

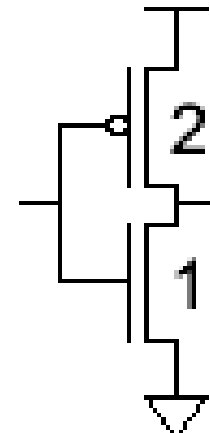
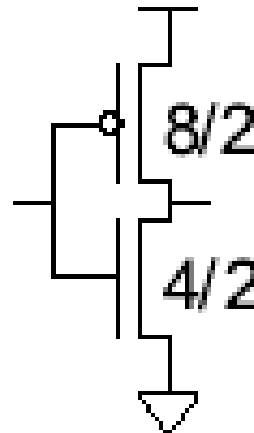
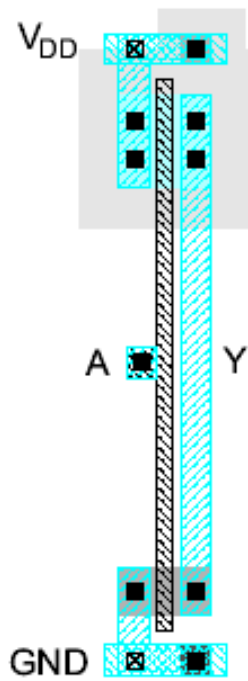
Simplified Design Rules

- ❑ Conservative rules to get you started



Inverter Layout

- ❑ Transistor dimensions specified as Width / Length
 - Minimum size is $4\lambda / 2\lambda$, sometimes called 1 unit
 - For $0.6\ \mu\text{m}$ process, $W=1.2\ \mu\text{m}$, $L=0.6\ \mu\text{m}$



Summary

- ❑ MOS Transistors are stack of gate, oxide, silicon
 - ❑ Can be viewed as electrically controlled switches
 - ❑ Build logic gates out of switches
 - ❑ Draw masks to specify layout of transistors
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- ❑ Now you know everything necessary to start designing schematics and layout for a simple chip!