Tutorial Assignments: Analog Signal Processing (EE60032),

Department of Electrical Engineering, Indian Institute of Technology, Kharagpur

Faculty: Ashis Maity Session: Autumn 2018

1. A current mirror circuit is shown in Figure 1 where I_{in}=100 µA and each transistor has W/L = 10µm/0.4µm. Find out the output impedance (r_{o2}) and the input impedance ($1/g_{m1}$). Also estimate the change in I_{out} for a 100 mV change in the output voltage. What voltage must be maintained at the drain of M_2 to ensure it remains in active mode? Assume: λL= 0.16 µm/V and μC_{ox} = 190 µA/V^2.

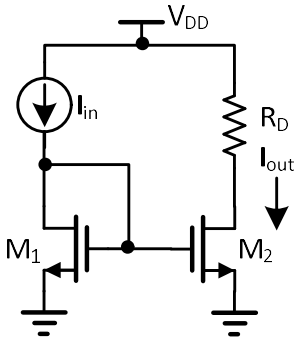

Figure 1

2. Design an NMOS differential pair with resistive load (shown in Figure 2) for a voltage gain of 5 and a power budget of 2mW subject to the condition that the stage following the differential pair an output CM level of at least 1.6V. Assume: $\mu_n C_{ox}$ = 100 µA/V^2, λ=0 and V_{DD} = 1.8 V.

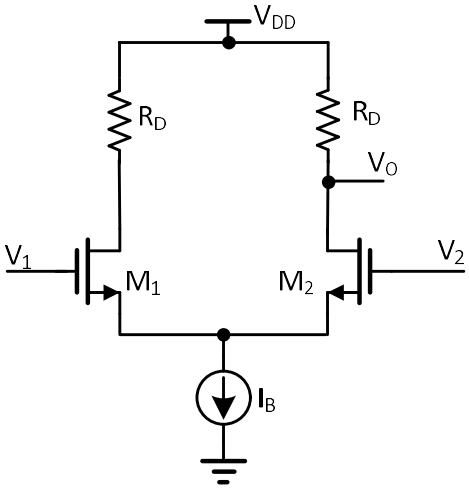

Figure 2

3. A differential amplifier with an active current mirror load (shown in Figure 3) has a tail bias current of 200 µA. All the transistors have W/L = 20µm/0.4µm. Find the output impedance r_{out} and the differential gain of the circuit. Assume: λL= 0.16 µm/V and μC_{ox} = 190 µA/V^2.

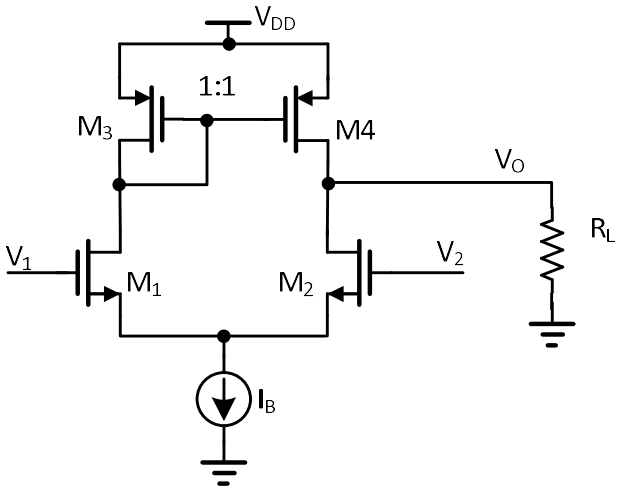

Figure 3

Answers:

1. r_{o2}= 25kohms; $1/g_{m1}$ = 1.03kohms ; Δ I_{out} = 4 µA ; V_{eff2} = 205 mV
2. R_D = 360 ohms ; W/L = 1738 ; I_{ss} = 1.11 mA