PSpice Assignments 1: Analog Signal Processing (EE60032),

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Faculty: Ashis Maity Session: Autumn 2018

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Submission procedure: Take the snapshot of the schematic and save the waveforms and prepare a word document. Add comments/discussion wherever required. The whole report should not exceed six pages. Submit the hard-copy/print-out version of the report.

1. A current mirror circuit is shown in Figure 1 where I_{in}=100 µA.
   a. Find out the threshold voltage of the transistors.
   b. If each transistor has W/L = 10µm/0.5µm, measure the value of I_{out}.
   c. After that, increase the transistor size 100µm/5µm and measure the value of I_{out}.
   d. Are there any differences you see in the results in step (b) and step (c)? Comment.

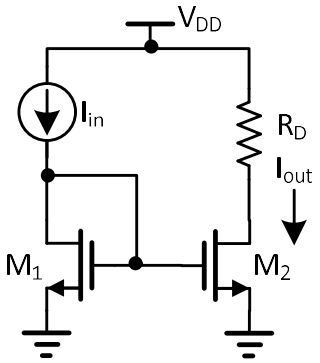

Figure 1

2. Design an NMOS differential pair with resistive load (shown in Figure 2) for a voltage gain of 50 and a power budget of 200 µW subject to the condition that the stage following the differential pair an input CM level of at least 1.2V.

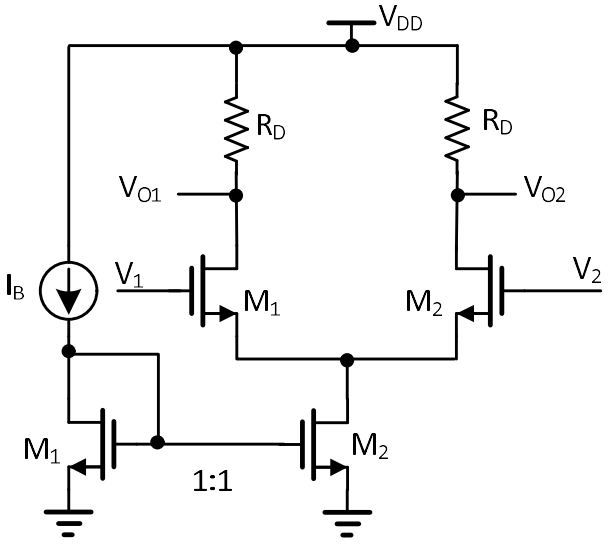

Figure 2

3. A differential amplifier with an active current mirror load (shown in Figure 3) has a tail bias current of 200 µA. All the transistors have W/L = 20µm/0.4µm. Assume the input common mode voltage of 1.2 V and R_L=10 kΩ.
    a. Find out the differential gain of the circuit.
    b. Find out the output common mode range.

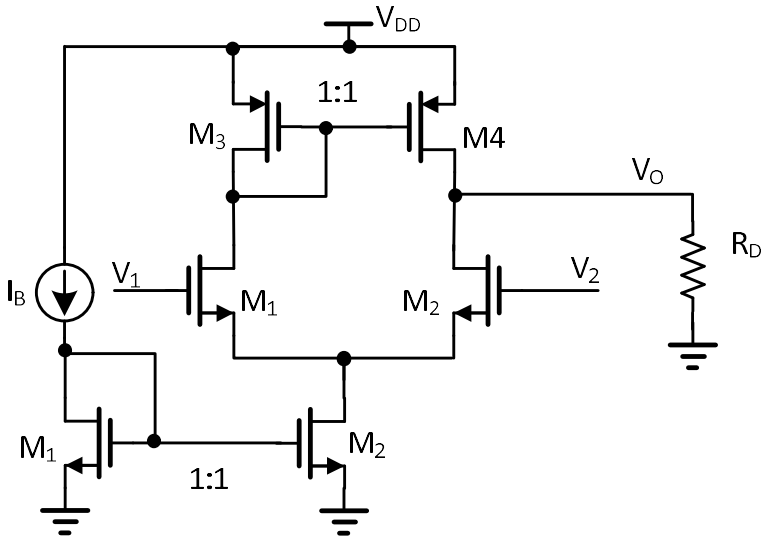

Figure 3