Design Assignments in Cadence: Mixed Signal Circuits and Systems-on-Chip (EE60100)

Department of Electrical Engineering, Indian Institute of Technology, Kharagpur

Faculty: Ashis Maity Session: Spring 2020

Submission Guidelines:

- Only the soft copy of the report is acceptable. Soft copy should be sent to **springee60100@gmail.com** on or before **15th March 2020**.
- Do not write unnecessary things. The report should be limited to 2 pages per problem.
- Do NOT copy the design and report from others. If found, both will be penalised.

Full Marks: 10X3=30

a) Design a push-pull output comparator to meet the following specifications: DC gain = 35 dB, Total Quiescent current consumption < 100µA, Load capacitance = 0.5 pF.
Report the following: ¬
   a) Your design path in the server.
   b) Snap-shot of cadence Schematic with node voltages. (Extra credit will be given for drawing neatly like book/paper quality)
   c) Table: All transistors (W/L).
   d) DC gain plot and value of unity gain frequency.
   e) Show a transient response with ±20mV and report the settling time
   f) Find out the ICMR range from your design.

2. Using the push-pull output comparator, now modify the circuit to get a hysteresis band of ±50mV.

Report the following:¬

   a) Your design path in the server.
   b) Snap-shot of cadence schematic. (Extra credit will be given for drawing neatly like book/paper quality)
   c) Table: All transistors (W/L).
   d) Hysteresis plot.
   e) Show a transient response with ±100mV triangular waveform having a frequency of 100 kHz.

3. Design a rail to rail comparator using constant gm input stage and meet the following specifications: DC gain = 60 dB, Total Quiescent current consumption < 200µA, Load capacitance = 0.5 pF.

Report the following: ¬

   a) Your design path in the server.
   b) Snap-shot of cadence Schematic with node voltages. (Extra credit will be given for drawing neatly like book/paper quality)
   c) Table: All transistors (W/L).
   d) Sweep the input common mode voltage Vin,CM from 0 to VDD and plot the input transistors' (PMOS as well as NMOS) currents.
   e) DC gain plot and value of unity gain frequency at Vin,CM=500 mV, Vin,CM=VDD/2 and Vin,CM=(VDD-500mV) .
   f) Show a transient response with ±20mV and report the settling time.