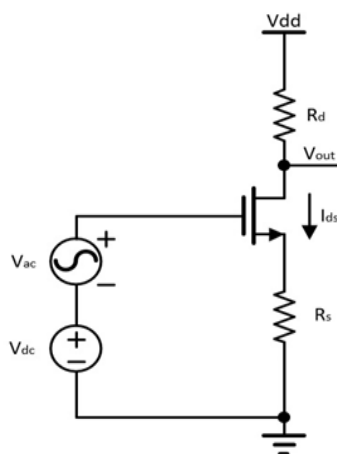


Submission Guidelines:

- ✓ Only the soft copy of the report is acceptable. Soft copy should be sent to **springee60100@gmail.com** on or before **3rd February 2020**.
- ✓ Do not write unnecessary things. The report should be limited to 2 pages per problem.
- ✓ Do NOT copy the design and report from others. If found, both will be penalised.

Full Marks: 10X2=20

1. Design a common source amplifier with source degeneration to meet the following specification: $V_{dd}=1.8\text{ V}$, $I_{ds}=50\text{ }\mu\text{A}$, $\mu_n C_{ox}=580\text{ }\mu\text{A/V}^2$, $V_{th}=380\text{ mV}$, $R_s=5\text{ k}\Omega$, output swing= 1 - 1.8 V. Use 1.8 V transistors for your design.



Report the following: -

- a) Your design path in the server.
 - b) Snap-shot of cadence Schematic with dc node voltages. (Extra credit will be given for drawing neatly like book/paper quality)
 - c) Table: aspect ratio of transistors (W/L), R_d , g_m .
 - d) Show the gain and phase plot from 0.001 Hz to 1 GHz.
2. Design a differential amplifier with current mirror load to meet the following specification:
 $V_{DD}=1.8\text{ V}$, $I_B(\text{tail current})=50\text{ }\mu\text{A}$, $0.8\text{ V} \leq \text{ICMR} \leq 1.6\text{ V}$, small signal gain=30 dB, with $C_O(\text{Load capacitor})=1\text{ pF}$. Use 1.8 V transistors for your design.

Report the following: -

- a) Your design path in the server.
- b) Snap-shot of cadence schematic with dc node voltages. (Extra credit will be given for drawing neatly like book/paper quality).
- c) Table: All transistors (W/L).
- d) Show the gain and phase plots from 0.001 Hz to 1 GHz at two different input common mode levels of 0.8 V and 1.6 V.
- e) Find the value of unity gain frequency.
- f) Find the output common mode range of your design.